AMENDMENTS TO THE CLAIMS

Please amend claims 1, 3, 4 and 8 in accordance with the following list of claims:

1. (Currently Amended) A semiconductor chip package comprising:

a first integrated semiconductor chip having a one side and a reverse ~~side;~~ side, and having a first electrode for wiring ~~formed~~ on the first chip one side;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface;

a second integrated semiconductor chip having a one side and a reverse side, and having a second electrode for wiring on the second chip on side, the second chip being mounted on the interposer substrate first surface with the second chip one side facing the interposer substrate first ~~surface; and~~ surface, such that the ~~a~~ second electrode ~~for wiring formed on the second chip one side so as to be~~ is exposed through the through-hole, the second electrode to be wired through the through-hole to external terminals on the interposer substrate second surface,

the first chip being mounted on the second chip reverse side with the first chip reverse side facing the second chip reverse side.

2. (Canceled)

3. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, ~~size and~~ having a one side and a reverse ~~side;~~ side, and having a first electrode for wiring ~~formed~~ on the first chip one side;

a second integrated semiconductor chip having a second chip size, ~~size and~~ having a one side and a reverse side, and having a second electrode for wiring on the second chip one side, the first chip being mounted to the second chip with the second chip reverse side facing the first chip reverse side;

~~a second electrode for wiring formed on the second chip one side;~~

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface,

the through-hole being larger than the second chip size;

an adhesive sheet having opposite first and second surfaces, the adhesive sheet being formed of a sheet-shaped adhesive material provided on the interposer substrate at the interposer substrate first surface so as to cover the through-hole, the adhesive sheet second surface being exposed through the through-hole from a side of the interposer substrate at the interposer substrate second surface,

wherein the second chip reverse side is fixed to the adhesive sheet second surface, and the first chip reverse side is fixed to the adhesive sheet first surface so as to face the second chip reverse side at a position at which the second chip is fixed, whereby the second electrode can be wired to external terminals on the interposer substrate second surface.

4. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, ~~size and~~ having a one side and a reverse ~~side;~~ side, and having a first electrode for wiring ~~formed~~ on the first chip one side;

a second integrated semiconductor chip having a second chip size and having a one side and a reverse side, the first chip being mounted to the second chip with the second chip reverse side facing the first chip reverse side;

an interposer substrate having a through-hole, the through-hole being smaller than the first chip size and larger than the second chip size,

wherein the first chip is mounted on the interposer substrate first surface at a portion of the first chip reverse side, such that the through-hole is covered by the first chip, and

wherein the second chip reverse side is fixed to the first chip reverse side, the first chip reverse side being exposed through the through-hole from a side of the interposer substrate at the interposer substrate second surface.

5. (Previously Presented) A semiconductor chip package according to claim 1, wherein the interposer substrate has a sunken region, which is sunken into the side of

the interposer substrate at the interposer substrate second surface, and the through-hole is provided through the sunken region.

6. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate has, a sunken region, which is sunken into the side of the interposer substrate at the interposer substrate second surface, and the through-hole is provided through the sunken region.

7. (Previously Presented) A semiconductor chip package according to claim 4, wherein the interposer substrate has a sunken region, that is sunken into the side of the interposer substrate at the interposer substrate second surface, and the through-hole is provided through the sunken region.

8. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, ~~size and~~ having a one side and a reverse ~~side;~~ side, and having a first electrode for wiring ~~formed~~ on the first chip one side;

a second integrated semiconductor chip having a second chip size, ~~size and~~ having a one side and a reverse side, and having a second electrode for wiring on the second chip one side, the first chip being mounted to the second chip with the second chip reverse side facing the first chip reverse side;

~~a second electrode for wiring formed on the second chip one side;~~

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface; and

an adhesive sheet formed of sheet-shaped adhesive material at the interposer substrate first surface so as to cover the through-hole, the adhesive sheet being larger than the second chip size and having a hole smaller than the second chip size,

wherein the second chip is fixed, at the second chip one side, to the interposer substrate first surface via the adhesive sheet, and

wherein the second electrode for wiring is exposed from the side of the interposer substrate at the interposer substrate second surface through the adhesive sheet small hole and the interposer substrate through-hole.

9. (Previously Presented) A semiconductor chip package according to claim 1, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

10. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

11. (Previously Presented) A semiconductor chip package according to claim 4, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

12. (Previously Presented) A semiconductor chip package according to claim 8, wherein the interposer substrate is formed of one of a nonconductive tape and a glass epoxy material.

13. (Previously Presented) A semiconductor chip package according to claim 3, wherein both surfaces of the adhesive sheet become viscous when heated.

14. (Previously Presented) A semiconductor chip package according to claim 8, wherein both surfaces of the adhesive sheet become viscous when heated.

15. (Previously Presented) A semiconductor chip package according to claim 8, wherein the interposer substrate has external terminals on its second surface to which the

second electrode can be wired, and external terminals on its first surface to which the first electrode can be wired.

16. (Previously Presented) A semiconductor chip package according to claim 15, further comprising:

a plurality of solder balls mounted to the interposer substrate second surface, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

17. (Previously Presented) A semiconductor chip package according to claim 4, wherein the interposer substrate has external terminals on its second surface to which the second electrode can be wired, and external terminals on its first surface to which the first electrode can be wired.

18. (Previously Presented) A semiconductor chip package according to claim 17, further comprising:

a plurality of solder balls mounted to the interposer substrate second surface, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

19. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate has external terminals on its first surface to which the first electrode can be wired, and the semiconductor chip package further comprises a plurality of solder balls mounted to the interposer substrate second surface, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

20. (Previously Presented) A semiconductor chip package according to claim 1, wherein the interposer substrate has external terminals on its first surface to which the first electrode can be wired, and the semiconductor chip package further comprises a plurality of solder balls mounted to the interposer substrate second surface, the solder balls being

electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.